



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of: Cho et al.
Patent No.: 7,085,154
Issued: Aug. 1, 2006
Atty. Docket No.: SAM-0519
Title: Device and method for pulse width control in a phase change memory device

SUBMISSION OF PRIOR ART UNDER 37 C.F.R. §1.501

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5/25/11
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir or Madam:

The undersigned herewith submits in the above-identified patent the following prior art which is pertinent and applicable to the patent and is believed to have a bearing on the patentability of at least claims 1, 2, 5, 6, 20, 26, 27, 30, and 31:

Rose et al., US 5,541,869, Jul. 30, 1996

Rose et al. anticipates at least claims 1, 2, 5, 6, 20, 26, 27, 30, 31 of US 7,085,154 B2 under 35 USC 102(b) as follows:

Regarding claim 1, Rose et al. discloses a method of programming a semiconductor memory device (amorphous silicon is the active material of a synaptic memory device, column 3, lines 34-44), comprising: applying a set pulse continuously to the memory device (column 2, lines 51-55), applying the set pulse to the memory device comprises applying a current to a bit line of the memory device (although a “bit line” is not explicitly shown the memory device is suggested to be addressed in an array which inherently implies such a bit line, see column 1, lines 57-60, column 3, lines 20-23); while the set pulse is applied, detecting a state of the memory device (column 2, lines 51-55 teaches measurement of the state after each pulse); and when the memory device is determined to be in a desired set state, removing the set pulse by removing the current applied to the bit line of the memory device, such that duration of the set pulse is controlled based on the state of the memory device (column 2, lines 56-57 teaches terminating the pulse

series based on the resistance state).

Regarding claim 2, Rose et al. discloses when the memory device is in a reset state, a programmable material of the memory device is in an amorphous state (amorphous silicon, column 3, lines 35-44).

Regarding claim 5, Rose et al. discloses detecting a state of the memory device comprises detecting a resistance in the device (column 2, lines 51-55).

Regarding claim 6, Rose et al. discloses the detected resistance comprises resistance in a programmable material of the memory device (column 1, lines 56-57).

Regarding claim 20, Rose et al. discloses applying a set pulse to the memory device comprises generating a control signal which controls application of the set pulse to the memory device (this is implied by the method of column 2, lines 49-61).

Regarding claim 26, Rose et al. discloses a semiconductor memory device (amorphous silicon is the active material of a synaptic memory device, column 3, lines 34-44), comprising: a detecting circuit for detecting a state of the memory device (this is inherent from column 2, lines 51-55 which teaches measurement of the resistance after each pulse); and a controller for continuously applying a set pulse to the memory device by continuously applying a current to a bit line of the memory device (this is inherent from column 2, lines 51-55 which teaches applying a series of pulses to the memory device), the controller removing the set pulse when the memory device is detected to be in a desired set state, such that duration of the set pulse is controlled based on the state of the memory device (column 2, lines 56-57).

Regarding claim 27, Rose et al. discloses a programmable material, wherein, in a first state, the programmable material is in an amorphous state (amorphous silicon is used as the programmable material, column 3, lines 35-44).

Regarding claim 30, Rose et al. discloses that the detecting circuit detects a resistance in the device (column 2, lines 51-55).

Regarding claim 31, Rose et al. discloses that the detected resistance comprises resistance in a programmable material of the memory device (column 1, lines 55-56).

CERTIFICATE OF SERVICE

I hereby certify on Oct.27, 2010, that a true and correct copy of the foregoing "Submission of Prior Art" was mailed by first-class mail, postage paid, to:

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CONCLUSION

For the reasons presented above Rose et al., which was not cited during the patent examination of US 7,085,154, is seen to have bearing on the patentability of claims 1, 2, 5, 6, 20, 26, 27, 30, and 31 of US 7,085,154 as prior art.

All correspondence may be made to the following address:

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Respectfully Submitted,



Blaise Mouttet



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